Simultaneous Logic Operation Using Optical Shadow Casting Technique for 3D Scheme

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Abstract—This paper represents the fastest operations in parallel processing of logical units, free space interconnection using the non-polarized characteristics of light. Different new algorithms are exploited in the design of optical computing modules using encoded optical shadow casting (OSC) scheme. In advanced VLSI system 3D IC is one of the hosts of 3D integration schemes that use the z direction to gain the higher electrical performance. In order to achieve more functionality within a compact space, 3D IC is structured by bracing silicon wafers and interconnects them vertically using through-silicon via (TSV) technique, as such they can behave like a system on chip (SOC). As this is a new technology, people will face new hardship or obstacles including cost, yield, heat, design complexity and interconnects however lack of standards. Interconnection problem is relatively dreadful in this 3D IC system whereas we can possess a free space interconnection 3D system, the generalized OSC design algorithm which realizes a functional truth table is used to design parallel logic gates. In this paper we evolve a new design scheme for parallel processing of logical units that shallows less power, less area and massive improvement in parallel interconnection. This design of parallel OSC demonstrates a completely novel computing system as it is capable of triggering to compute parallel logical operation of the two bit binary variables. The design algorithm for identity the source patterns, input encoding pattern and output decoder with possible parallel implementation are also presented. This design efficiency improves up to 77.78% compared to the conventional design algorithms.

Keywords— VLSI, 3D IC, Parallel processing, OSC, Logic, Optics, Fast processing.

1. INTRODUCTION

Faster, cooler and smaller system design is the biggest demand in this century for advanced technology. By diminishing the size of electronic components to a very small Nano-size scale, the speed of computers has been achieved. However they are not only limited by the speed of electrons in matter but also with increasing density of interconnections necessary to link the electronic gates on micro-chip[2]. Conventional 2D ICs have transistors formed on the top surface of the semiconductor wafer. In order to build 3D IC additional semiconductor layers are needed on top of existing devices and interconnect layers. Moreover there are some crucial prerequisites for the layer of 3D formation. The first precedentis defect free single crystalline semiconductor layer. The second one is lower temperature processing in order to avoid disturbance of existing devices and interconnect lines underneath and forming 3D layer.3D formation is arduous since it's practically nonviable single crystalline semiconductor on top of amorphous layers. However, Optics possesses a free space interconnection based computing system where photons are used in the place of electrons. Moreover an electronic computer is not competent to perform large amount of data in parallel because of a fundamental inadequacy [2]. Conventional 2D system accomplish instructions lead by a program counter step by step and access the data to/from a register from/to the memory sequentially.

This processing prevents us from the implementation of high speed computing system. Compare to serial computing, parallel computing is much better suited for modeling simulating and understanding, complex real world phenomenon. One initiative to get over this bottleneck is electronic computing that compute or execute a huge data processing at a rate which is much higher than those of the existing digital computers [1]. Computing system development rely on a fully parallel architecture of a system[3,4].In spite of that, the development of a fully parallel computing system is grueling on account of operational and technical problems related to complexity of interconnections of parallel processing component and algorithms that cannot steer parallel processing efficiently. So another propitious solution of this interconnection bottleneck is to build up an optical computing system that is capable of computing parallel operations in free space interconnection. Optics contemplated as one of the most promising techniques of new computing system and has following features that are unrealizable in the electronic computing system [5, 6].

- No short circuits, light beam can cross each other without interfacing with each other's data.
- Higher parallelism, less loss in communication, massive improvement in highly parallel computation such as image processing which is discussed in Section 4.
- Coupling between the input and output is less difficult than with the electronic system.

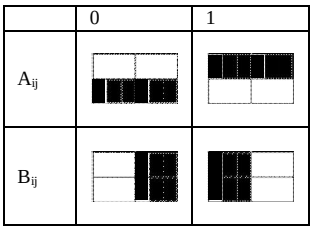
The inherent parallel processing was often highlighted as one of the key advantage of optical processing compared to the electronic processing using computers. Therefore, Optics has an important potential for processing large amount of data in real time. Optical computing or else known photonic computing uses photon generated by lasers or LED for computation. This parallelism helps in staggering computational power.

This paper presents the modified algorithms of OSC that is used to design and implement parallel logical operation using the features of non-polarized optical shadow casting method. It also illustrates the efficiency improved up to 77.78 percent through the modified design algorithm compare to the previously developed OSC scheme.

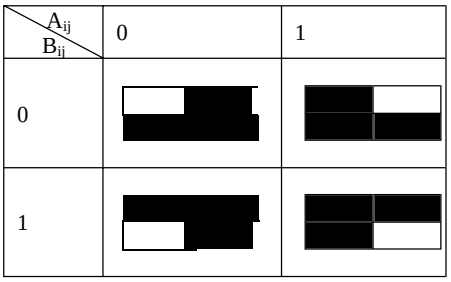
2. OPTICAL SHADOW CASTING METHOD

The processing speed of 3D IC is constitutionally limited by the interconnection gridlock. Parallel computer architectures also hindered by bus constraints and channel bandwidth [7]. To make a paradigm shift in computing system optics should be heeded to overcome the limitations aligned with electronic computing. Several distinct techniques have been proposed for implementing numerous algorithms in Optical shadow casting (OSC) method. Optical Shadow casting technique renders several data processing and other operations in parallel much faster and in an easier way than electrons. The assumption of OSC technique for implementing two-operand optical logic gates has been first proclaimed by Tanida and Ichioka [1].

The system is capable of performing the 16 logical operation associated with two binary variables. Basically the elements of OSC are one set of LED, an input transparent overlap cells which is called encoded input cell and an output decoding mask. Consider an input binary image composed of N*N small square areas. Each small box is counted as a cell. The values of all the cells are coded into a pattern composed of black and white rectangles. In this route, the values of cells in input image A are encoded, then input image B is also encoded in a similar manner Fig. 1(a). The encoded input patterns (A, B) are overlapped over each other for achieving 4 combination logics AB, A'B, AB', A'B'. However the ij cell in the input plane is encoded by any one of the four patterns in Fig.1 (b) .Where the white portion of the ij cell is transparent and the hatched portion is opaque. The light propagating from the LED set will pass through the transparent portion and hence imposed on the output decoding mask. The Decoding mask will extract the true outputs [1]. This coding method of the input image and the manner of overlay of the coded images shown in Fig.2 which represents an important role in realizing parallel logic operations of two binary variables using the optical shadow casting technique.



(a)



(b)

Fig.1 (a) coding of two binary variables (b) overlay of the two coded patterns.

The input pattern of A for logic 1 is encoded as a horizontal opaque and transparent stripe pattern and for logic 0 is just the inverse. Hence for logic 1, the input pattern of B is encoded as a vertical opaque and transparent stripe pattern while logic 0 being the opposite. The input logics 0 and 1 are introduced by transparent and opaque cells respectively and the coding procedures provides four AND overlapping operation, that is AB, A'B, AB', A'B' simultaneously as shown in Fig. 1(b).These products are called the minterms. This superimposed image is the input coded image of the optical logic array processor and set in the input plane. Four spatially distributed LEDs are dedicated to illuminate the encoded input, that causes 9 pixels shadow casting on the output decoding plane.

For an example if we consider XOR logic, the combination of LEDs should be:

L_{11}=Off, L_{12}=On, L_{21}=On and L_{22}=Off as XOR function is expressed as: F=a' b + a b'

From this expression it is perceive that in this gate a bright output in the boxed area has to be given only when the value of the ij cell in either of input images A or B is true. This occurs when L_{12} and L_{21} LEDs are switched to the ON state and L_{11} and L_{22} LEDs are switched to the OFF state. From simple geometrical consideration it is clear that the boxed area in the central part of the superposition of the projections of the ij cell represents the XOR configuration with bright-true-logic [1]. Fig. 2 shows this scenario for the combinational logic 01.

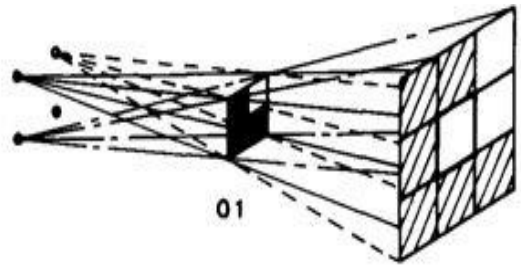


Fig.2 3D free space interconnect optical system for XOR operation

3. MODIFIED DESIGN ALGORITHM

A. *Parallel OSC Algorithm*

Conventional OSC method can demonstrate only one logic function at a time as it gets one logic output using one LED set. However to implement the logical operations in parallel, more than one output must be extracted from one decoding mask for each set of LED pattern. An OSC design scheme involves determining the source LED pattern, the encoding patterns of the input and the decoding mask which will yield the desire output of logic unit in parallel is described as follows:

Step 1: Two input pattern must be determined for logical operations. As we kept the input pattern same as like the conventional OSC input patterns. Fig. 1 shows the schematic diagram of the input pattern A and B. The input pattern A and B are the combination of 2×2 small areas where each area is known as cell. Here each cell is specified by ij co-ordinations.

The size of input block = 2 pixel length by 2 pixel width (2×2)

Step 2: The two encoded binary images are overlapped to cover the corresponding cells with each other. Fig. 1(b) shows the coded patterns in a manner corresponding to the combination (Aij, Bij) = (0, 0), (0, 1), (1, 0), (1, 1)

Input encoding overlapped pattern = 2 pixel length by 2 pixel width (2×2).

Step 3: An OSC design accommodate input patterns, the LED source pattern and one decoding mask. In conventional OSC [1] with one set of source LEDs produce one output at a time. For example Fig. 3(a) shows the source LED pattern for A+B function.

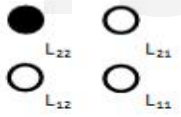


Fig. 3(a) source LED pattern for (A+B) logic

In conventional OSC methodology, with this pattern merely one logic output can be determined from O22 cell of output panel.

Step 4: In order to attain the parallel processing operation with this pattern if we correlate the output of each cell of the block with the truth table we can get (A+B)', A', A'B, B', A+B, AB, AB' and F (false) functions from different output position using operation this one set of LEDs. The output decoding mask for this parallel logical operation is shown in Fig. 3(b)

(A+B)'	A'	A'B
B'	A+B	AB
AB'		0

Fig.3 (b) output decoding mask for parallel processing logical units

Size of output block for 8 outputs = 3 pixel length by 3 pixel width (3×3)

Modified Design Efficiency:

This modified design re-uses the same LED pattern for generating different logical units to adjacent cell which is 77.78% more efficient than conventional design. In this design the average number of pixels per output is 9/8 or 1.125 and average number of LEDs per output is 4/8 or 0.5. The average number of pixels and LEDs per output in this design is 8 times lower than the conventional design which makes the design efficiency much higher than the conventional one. However the input pattern and LED pattern are same for both designs.

The overlap equations for each output generation:

(A+B)'= L11 (A'B'); [for O11 cell]
A'= L12 (A'B') + L11 (A'B); [for O12 cell]
A'B= L12 (A'B); [for O13 cell]
B'= L21 (A'B') + L11 (AB'); [for O21 cell]
A+B= L21 (A'B) + L12 (AB') + L11 (AB); [for O22 cell]
AB= L12 (AB); [for O23 cell]
AB'= L21 (AB'); [for O31 cell]
0=L22; [for O33 cell]

B. *Overlapping Method*

In previous section only one set of LEDs has been used to extract 8 logical outputs in parallel. In addition to get more logical functions the number of LED sets have to be increased and placed next to the previous set and output screen must be overlapped with each other edge cell. Single edge column cell of the two decoding masks are overlapped with each other as shown in Fig. 4.

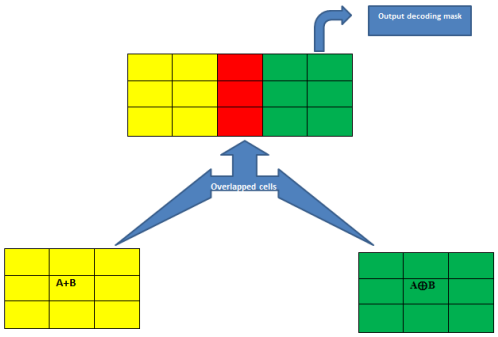


Fig.4 overlapping decoding mask

From Fig. 4 the decoding mask have 15 cells whence we can extract 10 logical functions in parallel by comparing the output of each cells and the truth table of the functions. For instance, if we overlap the output block of (A+B) and (A⊕B) in such a way that the distance between 2 sets of LED are in same as the distance between 2 LEDs in one set. Fig. 5 explains various outputs for two sets of LED combined together keeping the input pixel pattern unchanged.

input AB	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}
00	0	1	1	0	0	0	0	0	1	1
01	0	1	0	1	0	0	1	1	0	0
10	0	0	1	0	1	0	1	1	0	0
11	0	0	0	0	0	1	0	1	1	0
True Logic	F	A'	B'	A'B	AB'	AB	A⊕B	A+B	(A⊕B)'	(A+B)'

(c)

Fig. 5 (a) LED Source pattern (b) parallel logical outputs for Overlapping (A+B) and (A⊕B) (c) truth table of extracting 10 logical units

Conventional algorithms of OSC extract single output for each set of LED. So from LED patterns of (A+B) and (A⊕B) two outputs can be extracted as conventional manners. In contrast, after adding these both sets of LEDs to operate together along with overlapping their decoding screen we can extract different logical outputs for 00,01,10,11 inputs. Observe that the outputs for 00,01,10,11 inputs we obtain many other bright and dark states in parallel which is similar to those 10 logic's function. Fig.6. represents the parallel processing of logical units for those esteemed 10 logical functions.

				A'B
$\overline{B}$	A+B	$\overline{A \oplus B}$	A⊕B	
	AB	AB'		0

Fig. 6 logical outputs and decoding mask for overlapping (A+B) and (A⊕B)

However combining the 2 clusters together we can operate 10 functional parallel processing in addition with using less area for decoding mask and source input, less number of pixels and less number of LED sets as well as consuming less power hence constructing an efficient parallel processing unit.

Modified Design Efficiency:

1. Average number of pixels per output= 15/10
   = 1.5
2. Average number of LEDs per output= 8/10
   = 0.8
3. Modified design algorithm efficiency=10/15×100
   =66.67%

4. RELATED WORK AND COMPARISON

We have always made a paradigm shift in our technology to keep moving forward and keep advancing. Thus there is no doubt about the fact that in past 10 years, the renovation in transistor performance have been slowed down with the marginal power improvements from one process node to another, limiting the integration density .Multi-core parallel architectures have been developed to keep up with the demand [3,4].However to achieve their intend performance interconnect technology is inherently imperative in enabling these parallel new architectures. The limitation in the interconnect throughput, density and the discontinuation pose an extensive barrier to the performance of the system moreover hindering further approaches for future architecture. On the contrary the optically structured optical shadow casting system uses the light propagating in free space to wirelessly perform the logical functions and have the ability to perform parallel operations at the same time which is the predominant aspiration of our proposed design patterns.

The new technology 3D ICs address the scaling challenge by stacking 2D dies and connecting them in the 3rd dimension. This technology promises to speed up communication between layered chips, compared to planar layout [8]. 3D ICs pledge many remarkable benefits including power, design, cost, circuit security, heterogeneous integration, Bandwidth etc. However In 3D IC system, it faces some impediment like yield, heat, and design complexity as there are number of

Semiconductor layers where interconnection technology has to be employed precisely. It is very strenuous to create defect free interconnection. Thus using optical shadow casting these flaws can be solved.

The scope of optical shadow-casting was broadened by polarization encoded optical shadow casting technique. Additional design variables polarized pixel codes have been introduced for encoding the source, input and the decoding mask. The geometry of the POSC scheme is identical as OSC technique. But the design scheme of POSC is much more complex than the Non-Polarized OSC as it is necessary to use four different masks i.e. , vertically polarized, horizontally polarized, mixed polarized and true mask to identify the 4 different outputs based on their intensity in the output. [9] On the other hand, in our proposed OSC design we have to count only the cell state, whether it is transparent (true logic) or opaque (false). Moreover, OSC features have more advantages compare to the POSC schemes as consuming less power, cost effective and in inference problem.

In the field of optical parallel digital computing, Tanida and Ichioka have established the standards and roadmap of Optical shadow casting technique. In [1] the OSC technique, the system realizes two-operand logic gates and capable of performing the 16 logic functions associated with two binary variables. To perform the 10 logical operations in parallel according to [1] we have to implement or use 16 sets of LED as source input and (10×9)=90 pixels for output decoding screen. Hence in our 1st proposed design (section 4A), we used 1set of LED as source input and 9 pixels for output decoding screen for extracting 8 logical units in parallel and in 2nd proposed design(section 4B), we extract 10 logical units by using 2 sets of LED as source input and 15 pixels for output decoding screen.

5. DISCUSSION AND CONCLUSION

The Proposed design algorithms for OSC scheme is more versatile and Comprehensible, since it is free from polarization by electric field. In this paper, we designed 2 different new algorithms for parallel processing of logical units using less number of output decoding pixel, LED sets with new coding scheme which is respectively 77.78% (section 4A) and 66.67% (section 4B) efficient than the conventional OSC [1] scheme. The calculation of making new coding is unsophisticated. However design algorithms for cascading is still remain unperceived in OSC technique moreover increased density of operations per pixel needs extra measure of interference free system. Conventional electronic technology seems to be reaching its fundamental physical limits and therefore is unable to provide adequate architecture support for high speed and massively parallel processing. Due to inherent parallelism, high temporal bandwidths and no interfering communications, has the potential of breaking through the performance barriers faced by conventional technology and is therefore under serious consideration for implementing future high performance parallel processing design algorithms. The method presented here is one of initiatives to design the full Arithmetic and logical units with non-polarized OSC scheme in future.

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